ABSTRACT

MEMORY CONTROLLER

A memory controller, such as a SDRAM controller, controls the way in which data is retrieved, in order to make more efficient use of the bandwidth of the memory data bus. More specifically, when a memory access request requires multiple data bursts on the memory bus, the SDRAM controller stores the data from the multiple data bursts in respective buffers. Data is then retrieved from the buffers such that data is read from a part of the first buffer, then from the other buffers, and finally from the remaining part of the first buffer. Storing the required data in the remaining part of the first buffer avoids the need to occupy the memory bus with a new data burst.